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CANTOR COLBURN LLP - IBM FISHKILL  
55 GRIFFIN ROAD SOUTH  
BLOOMFIELD, CT 06002

EXAMINER

LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/711,084	Applicant(s) BUETI ET AL.	
	Examiner Christopher E. Lee	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 May 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2,10,11 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,10,11 and 20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                                                      |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                                                                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                                                 | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/20/04, 9/7/04</u> . | 6) <input type="checkbox"/> Other: _____                                                |

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the Amendment filed on 1<sup>st</sup> of May 2006. Claims 1, 10, 11, and 20 have been amended; claims 3-9 and 13-19 have been canceled; and no claim has been  
5 newly added since the Non-Final Office Action was mailed on 7<sup>th</sup> of February 2006. Currently, claims 1, 2, 10, 11, 12, and 20 are pending in this Application.

### *Information Disclosure Statement*

2. The information disclosure statements (IDS) were filed on 20<sup>th</sup> of August 2004, and on  
10 7<sup>th</sup> of September 2004. The submissions were in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements were considered by the Examiner in the Non-Final Office Action mailed on 7<sup>th</sup> of February 2006. However, as the Applicants noticed, the Examiner didn't initial on the individual references, accidentally. Therefore, the Examiner reconsiders the information disclosure statements in the instant Office Action.

15

### *Claim Objections*

3. Claims 1 and 11 are objected to because of the following informalities:

The claims 1 and 11 recite the subject matter "said external connections" in line 20 of the claim 1, and in line 21 of the claim 11, respectively. However, it has not been specifically  
20 clarified in the respective claims 1 and 11. Therefore, the Examiner presumes that the term "said external connections" could be considered as --external connections-- in light of the specification since it is not defined in the claims.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

5 (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10 5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later  
15 invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 2, 10, 11, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. [US 2005/0091432 A1; hereinafter Adams] in view of Simcoe et al. [US 5,265,257 A; hereinafter Simcoe], Zulian [US 5,941,967 A], Gappisch et al. [US  
20 2003/0033490 A1; hereinafter Gappisch], and Potter, JR. [US 2004/0187112 A1; hereinafter Potter].

*Referring to claim 1*, Adams discloses a system (i.e., System 500 in Fig. 6) for implementing arbitration between one or more shared peripheral core devices (i.e., Targets 515 of Fig. 6) in a system on chip (SOC) integrated circuit architecture (i.e., Matrix Fabric framework;

25 See paragraph [0051]), comprising:

- a first microprocessor (i.e., CPU1 507 of Fig. 6) in communication with a first system bus (i.e., Requestor Connection Port 520 between said CPU1 and Internal Switching Fabric 550 in Fig. 6);

- a second microprocessor (i.e., CPU2 508 of Fig. 6) in communication with a second system bus (i.e., Requestor Connection Port 520 between said CPU2 and Internal Switching Fabric 550 in Fig. 6);
- at least one peripheral core device (i.e., Targets 515, e.g., External Flash Controller 503, External SDRAM Controller 504, and Internal SRAM Controller 505 in Fig. 6) accessible by both said first microprocessor and said second microprocessor (See paragraphs [0052]-[0053]); and
- an arbitration unit (i.e., Internal Switching Fabric 550 of Fig. 6) in communication with said first system bus and said second system bus (See paragraphs [0058]-[0059]), said arbitration unit (i.e., said Internal Switching Fabric) configured to control communication between said at least one peripheral core device (i.e., said Targets) and said first and second microprocessors (i.e., arbitration control between CPUs and memory targets; See paragraph [0060]);
- said arbitration unit (i.e., said Internal Switching Fabric) further comprising:
  - a first buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU1 507 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said first system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection Port 520 between CPU1 507 and 3 Target Decoder/Router Element 502 in Fig. 6),
  - a second buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU2 508 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said second system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection

Port 520 between CPU2 508 and 3 Target Decoder/Router Element 502 in Fig. 6),

- input multiplexing circuitry (i.e., Routing Logic 405 of Fig. 5) in communication with said first buffer device, said second buffer device and said at least one peripheral core device (See Fig. 6 and paragraph [0046]); and
- arbitration logic (i.e., Arbiter 506 of Fig. 6) in communication with said first buffer device, said second buffer device and said input multiplexing circuitry (in fact, said Arbiter being communicated with said 3 Target Decoder/Router Element, which includes said Request Control Flow blocks and said Routing Logic; See paragraph [0052]); and
- said at least one peripheral core device (i.e., said External Flash Controller) further configured to communicate, at any time, data to and from (e.g., data read/write operation) the SOC integrated circuit architecture (i.e., said External Flash Controller communicating with off-chip Flash memory using Matrix Fabric framework at any time; See paragraphs [0058]-[0059]) through an associated external connection (i.e., request connection port 520 in Fig. 6) for each of said first and second microprocessors (i.e., said CPU1 and CPU2 in Fig. 6; See paragraph [0051]).

Adams does not expressly teach that said arbitration logic is configured to: detect a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors; determine the existence of a free peripheral from said at least one peripheral core device; and implement communication between a determined free peripheral and said requesting one of said first and second microprocessors.

Simcoe discloses a fast arbiter (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4; See Abstract and Fig. 4), wherein an arbitration logic (i.e., Resource Arbiter 10 of Fig. 4) is configured to:

- detect a request for access (i.e., Request 22 of Fig. 4) to at least one peripheral core device (i.e., Resources ID=1...n 16 in Fig. 4) by a requesting one of first and second microprocessors (e.g., one of Requesters ID=1 or m in Fig. 4; See col. 6, lines 22-26, and col. 14, lines 35-38);
- determine the existence of a free peripheral from said at least one peripheral core device (See col. 6, lines 26-33, and col. 14, lines 39-62); and
- implement communication (i.e., coupling said Requester to said Resource) between a determined free peripheral and said requesting one of said first and second microprocessors (See col. 6, lines 33-35, and col. 15, lines 1-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration of said fast arbiter (i.e., Resource Arbiter and Access Path Controller), as disclosed by Simcoe, in said arbitration unit, as disclosed by Adams, for the advantage of providing a capability of being easily scaled to both large number of processors (i.e., requesters) and large numbers of types of peripheral core devices (i.e., resources) where there are multiple instances of each type of peripheral core device (i.e., resource; See Simcoe, col. 3, lines 3-6).

Adams, as modified by Simcoe, does not teach that said arbitration logic is further configured to inform said requesting one of said first and second microprocessors whenever no free peripheral is presently available.

Zulian discloses a unit for arbitration of access to a bus of a multiprocessor system for access to a plurality of shared resources (See col. 1, lines 10-13), wherein

- an arbitration logic (i.e., arbitration unit) is configured to inform (i.e., sending RETRY signal) requesting one of first and second microprocessors (e.g., processor) whenever no free peripheral is presently available (i.e., temporarily unavailable; See col. 1, lines 21-52).

5 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said arbitration logic (i.e., arbitration unit), as disclosed by Zulian, in said arbitration logic, as disclosed by Adams, as modified by Simcoe, so as to informing (i.e., indicating) the state of said peripheral core devices (i.e., various resources) to said first and second processors (i.e., various requesting units; See Zulian, col. 1, lines 57-62), for the  
10 advantage of freeing busses (i.e., system bus) so as to make them available for other transactions rather than keeping said busses (i.e., system bus) busy until said peripheral core device (i.e., resource) becomes free (See Zulian, col. 1, lines 53-56).

Adams, as modified by Simcoe and Zulian, does not teach said arbitration unit further comprising external multiplexing circuitry in communication with said at least one peripheral  
15 core device and external connections.

Gappisch discloses a multiprocessor arrangements with shared non-volatile memory (See Abstract), wherein

- external multiplexing circuitry (i.e., multiplexer for said ADDRESS/DATA\_A and ADDRESS/DATA\_B in Fig. 1) in communication with at least one peripheral core device  
20 (i.e., Access Arbitration and Wait timer in Fig. 1) and external connections (i.e., ADDRESS/DATA\_A and ADDRESS/DATA\_B in Fig. 1; See paragraph [0013]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said external multiplexing circuitry (i.e., multiplexer for ADDRESS/DATA\_A and ADDRESS/DATA\_B), as disclosed by Gappisch, in said SOC



integrated circuit architecture (i.e., Matrix Fabric framework), as disclosed by Adams, as modified by Simcoe and Zulian, for the advantage of providing the improvement essentially by optimizing the synchronization between said first and second microprocessors (i.e., a plurality of microprocessors) and said at least one of peripheral core devices (i.e., one or more associated non-volatile or flash memories; See Gappisch, paragraph [0012]).

Adams, as modified by Simcoe, Zulian and Gappisch, does not teach said arbitration unit comprising an external buffer device coupled between said external multiplexing circuitry and said external connection.

Potter discloses a system for dynamic ordering in a network processor (See Abstract),

wherein

- an arbitration unit (i.e., Router/Switch 200 of Fig. 1) comprising an external buffer device (i.e., buffer and queuing unit 210 of Fig. 2) coupled between an external multiplexing circuitry (i.e., Selector Circuit 250 of Fig. 2) and an external connection (i.e., external connection 290 coupling external memory resources 280 in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dynamic ordering using said external buffer device (i.e., buffer and queuing unit and its control), as disclosed by Potter, in said arbitration unit, as disclosed by Adams, as modified by Simcoe, Zulian and Gappisch, for the advantage of maintaining a proper order among a plurality of data operations in said system (i.e., threads in a multi-threaded processing system; See Potter, paragraph [0011]).

*Referring to claim 2*, Adams teaches a plurality of arbitration units (i.e., Arbiters in Fig. 6; actually, internal Arbiter 506 within Internal Switching Fabric 550, and external Arbiters within Targets 515 in Fig. 6), wherein

- each of said plurality of arbitration units (i.e., each of said Arbiters) is configured to control communication between said first system bus and said second system bus (i.e., Requestor Connection Ports 520 in Fig. 6; See paragraph [0060]), and a group of peripheral core devices (i.e., Targets 515 in Fig. 6) associated therewith (i.e., Arbiter 506 associated with External Flash Controller 503, External SDRAM Controller 504 associated with its internal Arbiter, and Internal SRAM Controller 505 associated with its internal Arbiter in Fig. 6).

*Referring to claim 10, Simcoe teaches*

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) is configured to arbitrarily receive incoming data from one of said external connections (i.e., said Resource Arbiter receiving Resource Type 24 from one of Requesters ID=1...m in Fig. 4; See col. 6, lines 22-31) and identify a target destination (i.e., Resource ID) for said incoming data (See col. 6, lines 36-51);
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) is configured to internally note an assignment between a free peripheral (i.e., free instance Resource) and said target destination (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9); and
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) is configured to maintain said assignment until the completion of a completed data transfer between said one of said external connections (i.e., one of Requesters ID=1...m) and said target destination (i.e., Resource), through said free peripheral (See col. 6, lines 12-21 and col. 15, lines 18-26; i.e., wherein in fact that crossbar switch can be operated by the access path controller to immediately couple the particular requester to the particular resource while maintaining other couplings between different requesters and resources implies

that said arbitration unit is configured to maintain said assignment until the completion of a completed data transfer between said one of said external connections and said target destination, through said free peripheral, free instance device).

5        Referring to claim 11, Adams discloses a method (i.e., developing method for System 500 in Fig. 6; See paragraph [0003]) for implementing arbitration between one or more shared peripheral core devices (i.e., Targets 515 of Fig. 6) in a system on chip (SOC) integrated circuit architecture (i.e., Matrix Fabric framework; See paragraph [0051]), the method comprising:

- 10        • configuring a first microprocessor (i.e., CPU1 507 of Fig. 6) in communication with a first system bus (i.e., Requestor Connection Port 520 between said CPU1 and Internal Switching Fabric 550 in Fig. 6);
- configuring a second microprocessor (i.e., CPU2 508 of Fig. 6) in communication with a second system bus (i.e., Requestor Connection Port 520 between said CPU2 and Internal Switching Fabric 550 in Fig. 6);
- 15        • configuring at least one peripheral core device (i.e., Targets 515, e.g., External Flash Controller 503, External SDRAM Controller 504, and Internal SRAM Controller 505 in Fig. 6) to be accessible by both said first microprocessor and said second microprocessor (See paragraphs [0052]-[0053]); and
- configuring an arbitration unit (i.e., Internal Switching Fabric 550 of Fig. 6) in  
20        communication with said first system bus and said second system bus (See paragraphs [0058]-[0059]),
  - wherein said arbitration unit (i.e., said Internal Switching Fabric) controls communication between said at least one peripheral core device (i.e., said

Targets) and said first and second microprocessors (i.e., arbitration control between CPUs and memory targets; See paragraph [0060]);

- said arbitration unit (i.e., said Internal Switching Fabric) further comprising:
  - a first buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU1 507 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said first system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection Port 520 between CPU1 507 and 3 Target Decoder/Router Element 502 in Fig. 6);
  - a second buffer device (i.e., Request Control Flow block 403 of Fig. 5, which is actually located within 3 Target Decoder/Router Element 502 for CPU2 508 in Fig. 6; See paragraph [0046], lines 4-6) coupled to said second system bus (i.e., Requestor Connection Port block 101 of Fig. 5; in fact, Requestor Connection Port 520 between CPU2 508 and 3 Target Decoder/Router Element 502 in Fig. 6);
  - input multiplexing circuitry (i.e., Routing Logic 405 of Fig. 5) in communication with said first buffer device, said second buffer device and said at least one peripheral core device (See Fig. 6 and paragraph [0046]), and
  - arbitration logic (i.e., Arbiter 506 of Fig. 6) in communication with said first buffer device, said second buffer device and said input multiplexing circuitry (in fact, said Arbiter being communicated with said 3 Target Decoder/Router Element, which includes said Request Control Flow blocks and said Routing Logic; See paragraph [0052]); and

- said at least one peripheral core device (i.e., said External Flash Controller) further configured to communicate, at any time, data to and from (e.g., data read/write operation) the SOC integrated circuit architecture (i.e., said External Flash Controller communicating with off-chip Flash memory using Matrix Fabric framework at any time; See paragraphs [0058]-[0059]) through an associated external connection (i.e., request connection port 520 in Fig. 6) for each of said first and second microprocessors (i.e., said CPU1 and CPU2 in Fig. 6; See paragraph [0051]).

Adams does not expressly teach that said arbitration logic is configured to: detect a request for access to said at least one peripheral core device by a requesting one of said first and second microprocessors; determine the existence of a free peripheral from said at least one peripheral core device; and implement communication between a determined free peripheral and said requesting one of said first and second microprocessors.

Simcoe discloses a fast arbiter (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4; See Abstract and Fig. 4), wherein an arbitration logic (i.e., Resource Arbiter 10 of Fig. 4) is configured to:

- detect a request for access (i.e., Request 22 of Fig. 4) to at least one peripheral core device (i.e., Resources ID=1...n 16 in Fig. 4) by a requesting one of first and second microprocessors (e.g., one of Requesters ID=1 or m in Fig. 4; See col. 6, lines 22-26, and col. 14, lines 35-38);
- determine the existence of a free peripheral from said at least one peripheral core device (See col. 6, lines 26-33, and col. 14, lines 39-62); and

- implement communication (i.e., coupling said Requester to said Resource) between a determined free peripheral and said requesting one of said first and second microprocessors (See col. 6, lines 33-35, and col. 15, lines 1-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention

5 was made to have included said configuration of said fast arbiter (i.e., Resource Arbiter and Access Path Controller), as disclosed by Simcoe, in said arbitration unit, as disclosed by Adams, for the advantage of providing a capability of being easily scaled to both large number of processors (i.e., requesters) and large numbers of types of peripheral core devices (i.e., resources) where there are multiple instances of each type of peripheral core device (i.e.,  
10 resource; See Simcoe, col. 3, lines 3-6).

Adams, as modified by Simcoe, does not teach that said arbitration logic is further configured to inform said requesting one of said first and second microprocessors whenever no free peripheral is presently available.

Zulian discloses a unit for arbitration of access to a bus of a multiprocessor system for  
15 access to a plurality of shared resources (See col. 1, lines 10-13), wherein

- an arbitration logic (i.e., arbitration unit) is configured to inform (i.e., sending RETRY signal) requesting one of first and second microprocessors (e.g., processor) whenever no free peripheral is presently available (i.e., temporarily unavailable; See col. 1, lines 21-52).

20 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said arbitration logic (i.e., arbitration unit), as disclosed by Zulian, in said arbitration logic, as disclosed by Adams, as modified by Simcoe, so as to informing (i.e., indicating) the state of said peripheral core devices (i.e., various resources) to said first and second processors (i.e., various requesting units; See Zulian, col. 1, lines 57-62), for the

advantage of freeing busses (i.e., system bus) so as to make them available for other transactions rather than keeping said busses (i.e., system bus) busy until said peripheral core device (i.e., resource) becomes free (See Zulian, col. 1, lines 53-56).

Adams, as modified by Simcoe and Zulian, does not teach said arbitration unit further  
5 comprising external multiplexing circuitry in communication with said at least one peripheral core device and external connections.

Gappisch discloses a multiprocessor arrangements with shared non-volatile memory (See Abstract), wherein

- external multiplexing circuitry (i.e., multiplexer for said ADDRESS/DATA\_A and  
10 ADDRESS/DATA\_B in Fig. 1) in communication with at least one peripheral core device (i.e., Access Arbitration and Wait timer in Fig. 1) and external connections (i.e., ADDRESS/DATA\_A and ADDRESS/DATA\_B in Fig. 1; See paragraph [0013]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said external multiplexing circuitry (i.e., multiplexer for  
15 ADDRESS/DATA\_A and ADDRESS/DATA\_B), as disclosed by Gappisch, in said SOC integrated circuit architecture (i.e., Matrix Fabric framework), as disclosed by Adams, as modified by Simcoe and Zulian, for the advantage of providing the improvement essentially by optimizing the synchronization between said first and second microprocessors (i.e., a plurality of microprocessors) and said at least one of peripheral core devices (i.e., one or more associated  
20 non-volatile or flash memories; See Gappisch, paragraph [0012]).

Adams, as modified by Simcoe, Zulian and Gappisch, does not teach said arbitration unit comprising an external buffer device coupled between said external multiplexing circuitry and said external connection.

Potter discloses a system for dynamic ordering in a network processor (See Abstract),

wherein

- an arbitration unit (i.e., Router/Switch 200 of Fig. 1) comprising an external buffer device (i.e., buffer and queuing unit 210 of Fig. 2) coupled between an external multiplexing circuitry (i.e., Selector Circuit 250 of Fig. 2) and an external connection (i.e., external connection 290 coupling external memory resources 280 in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dynamic ordering using said external buffer device (i.e., buffer and queuing unit and its control), as disclosed by Potter, in said arbitration unit, as disclosed by Adams, as modified by Simcoe, Zulian and Gappisch, for the advantage of maintaining a proper order among a plurality of data operations in said system (i.e., threads in a multi-threaded processing system; See Potter, paragraph [0011]).

*Referring to claim 12, Adams teaches*

- a configuring plurality of arbitration units (i.e., Arbiters in Fig. 6; actually, internal Arbiter 506 within Internal Switching Fabric 550, and external Arbiters within Targets 515 in Fig. 6) to control communication between said first system bus and said second system bus (i.e., Requestor Connection Ports 520 in Fig. 6; See paragraph [0060]), and a group of peripheral core devices (i.e., Targets 515 in Fig. 6) associated therewith (i.e., Arbiter 506 associated with External Flash Controller 503, External SDRAM Controller 504 associated with its internal Arbiter, and Internal SRAM Controller 505 associated with its internal Arbiter in Fig. 6).



*Referring to claim 20, Simcoe teaches*

- said arbitration unit (i.e., Resource Arbiter 10 and Access Path Controller 20 in Fig. 4) arbitrarily receives incoming data from one of said external connections (i.e., said Resource Arbiter receiving Resource Type 24 from one of Requesters ID=1...m in Fig. 4; See col. 6, lines 22-31) and identifies a target destination (i.e., Resource ID) for said incoming data (See col. 6, lines 36-51);
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) internally notes an assignment between a free peripheral (i.e., free instance Resource) and said target destination (i.e., inputting requester ID and resource ID into said Access Path Controller; See col. 15, lines 3-9); and
- said arbitration unit (i.e., said Resource Arbiter and Access Path Controller) maintains said assignment until the completion of a completed data transfer between said one of said external connections (i.e., one of Requesters ID=1...m) and said target destination (i.e., Resource), through said free peripheral (See col. 6, lines 12-21 and col. 15, lines 18-26; i.e., wherein in fact that crossbar switch can be operated by the access path controller to immediately couple the particular requester to the particular resource while maintaining other couplings between different requesters and resources implies that said arbitration unit maintains said assignment until the completion of a completed data transfer between said one of said external connections and said target destination, through said free peripheral, free instance device).

***Response to Arguments***

7. Applicants' arguments filed 1<sup>st</sup> of May 2006 have been fully considered but they are not persuasive.

*In response to the Applicants' argument with respect to "With regard to the art of record,*

5 ... In addition, claims 1 and 11 further recite that the peripheral core device is able to communicate, at any time, data to and from the SOC integrated circuit architecture. Claims 10 and 20 have been amended ... The Examiner relies on the Gappisch reference as discloses multiprocessor arrangements communicating data through an external output path, and external multiplexing circuitry. However, the external device shown in the figures of Gappisch is flash  
10 memory. Because flash memory is a response-based device, it is therefore incapable of choosing when to send data to a requesting processor. This being the case, Gappisch therefore does not teach the peripheral core device being able to receive incoming external data at any time." in Response page 9, line 15 through page 10, line 3, the Examiner respectfully disagrees.

Actually, as the Applicants understood, a flash memory is a response-based device.

15 However, the peripheral core device, i.e., being mapped to Access Arbitration and Wait Timer in Fig. 1 of Gappisch, is able to receive incoming external data at any time (See Gappisch, paragraph [0013]).

Furthermore, in contrary to the Applicants' assertion, it is noted that the features upon which applicants rely (i.e., "choosing when to send data to a requesting processor" and/or "the  
20 peripheral core device being able to receive incoming external data at any time") are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, the Applicants' argument on this point is not persuasive.

8. Applicants' arguments with respect to claims 9, 10, 19, and 20 on pages 8-9 have been considered but are moot in view of the cancellation of the claims 9, 10, 19, and 20.

In fact, the Applicants concern about claims 1 and 11 rejection under 35 U.S.C. §112, first paragraph, because the claim language of cancelled claims 9 and 19, which have been rejected  
5 under 35 U.S.C. §112, first paragraph, appears in the amended claims 1 and 11, respectively (See Response on page 9, lines 11-14).

However, the scopes of the claimed invention in the amended claims 1 and 11 have been changed from the scope of the claimed invention in the cancelled claims 9 and 19, respectively, and the amended claims 1 and 11 comply with 35 U.S.C. §112, first paragraph.

10 Thus the claim rejection under 35 U.S.C. §112, first paragraph, is no more issue in the instant Office Action.

### ***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this  
15 Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after  
20 the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher E. Lee  
Patent Examiner  
Art Unit 2112

CEL/

